Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A process for manufacturing an integrated device, comprising the steps of:

forming a first conductive region;

forming an insulating layer which coats said first conductive region;

forming a through opening in said insulating layer above said first conductive region;

forming a contact structure ~~in~~ that covers sidewalls of said through opening and a portion of the first conductive region that defines a bottom of said through opening, said contact structure comprising a conductive material layer delimiting ~~a~~ an empty region that is open at a top end opposite to the bottom of said through opening; and

without previously depositing a filling material in the empty region, forming a second conductive region ~~above said through opening of said insulating layer~~that closes the top end of the empty region and delimits, together with the contact structure, the empty region~~;~~

~~wherein said region delimited by said contact structure is left empty~~.

2. (Original) The process for manufacturing an integrated device according to claim 1, wherein said conductive material layer is obtained by depositing a titanium layer.

3. (Original) The process for manufacturing an integrated device according to claim 2, wherein said titanium layer is deposited by PVD.

4. (Original) The process for manufacturing an integrated device according to claim 2 wherein said titanium layer has a thickness of between 10 and 100 nm.

5. (Original) The process for manufacturing an integrated device according to claim 1 wherein said conductive material layer is obtained by depositing a titanium-nitride layer.

6. (Original) The process for manufacturing an integrated device according to claim 5, wherein said titanium-nitride layer is deposited by CVD.

7. (Original) The process for manufacturing an integrated device according to claim 5 wherein said titanium-nitride layer has a thickness of between 50 and 200 nm.

8. (Original) The process for manufacturing an integrated device according to claim 1 wherein said step of forming said second conductive region comprises depositing conductive material in a non-conformal way over said region.

9. (Original) The process for manufacturing an integrated device according to claim 8, wherein said second conductive region contains platinum.

10. (Original) The process for manufacturing an integrated device according to claim 9 wherein said integrated device is a ferro-electric memory comprising a transistor and a ferro-electric capacitor; said step of forming a first conductive region comprises forming a first conduction region of said transistor in a substrate of semiconductor material; said step of forming an insulating layer comprises depositing insulating material on top of said substrate; and said step of forming a second conductive region comprises forming a first plate of said ferro-electric capacitor; the process further comprising forming a ferro-electric material region on top of said first plate, and forming a second plate of said ferro-electric capacitor on top of said ferro-electric material region.

11. (Currently Amended) A process for manufacturing an integrated device, comprising:

forming a first conductive region;

forming an insulating layer on the first conductive region;

forming a through opening in the insulating layer above the first conductive region;

forming a conductive material layer on walls of the through opening, the conductive material layer contacting the first conductive region, ~~and~~ surrounding an empty region, and having a top opening that exposes the empty region; and

without previously depositing a filling material in the empty region, forming a second conductive region ~~over~~ that closes the top opening and defines, together with the conductive material layer, the empty region~~, thereby closing the through opening and empty region~~.

12. (Original) The process for manufacturing an integrated device according to claim 11 wherein said conductive material layer is obtained by depositing a titanium layer.

13. (Original) The process for manufacturing an integrated device according to claim 12, wherein said titanium layer is deposited by PVD.

14. (Original) The process for manufacturing an integrated device according to claim 12 wherein said titanium layer has a thickness of between 10 and 100 nm.

15. (Original) The process for manufacturing an integrated device according to claim 11 wherein said conductive material layer is obtained by depositing a titanium-nitride layer.

16. (Original) The process for manufacturing an integrated device according to claim 15 wherein said titanium-nitride layer is deposited by CVD.

17. (Original) The process for manufacturing an integrated device according to claim 15 wherein said titanium-nitride layer has a thickness of between 50 and 200 nm.

18. (Original) The process for manufacturing an integrated device according to claim 11 wherein the through opening has a width of about 0.18 – 0.35 microns, forming the conductive material layer includes forming a first conductive layer having a thickness between 10 and 100 nm and forming a second conductive layer having a thickness between 50 and 200 nm.

19. (Original) The process for manufacturing an integrated device according to claim 18 wherein the first conductive layer includes titanium and the second conductive layer includes titanium nitride.

20. (Original) The process for manufacturing an integrated device according to claim 11 wherein said integrated device is a ferro-electric memory comprising a transistor and a ferro-electric capacitor; said step of forming a first conductive region comprises forming a first conduction region of said transistor in a substrate of semiconductor material; said step of forming an insulating layer comprises depositing insulating material on top of said substrate; and said step of forming a second conductive region comprises forming a first plate of said ferro-electric capacitor; the process further comprising forming a ferro-electric material region on top of said first plate, and forming a second plate of said ferro-electric capacitor on top of said ferro-electric material region.

21. (Currently Amended) A process of making an integrated device, comprising:

forming a first conductive region;

forming an insulating layer on the first conductive region;

forming a through opening extending in the insulating layer;

forming a contact structure in the through opening, the contact structure comprising a conductive material layer and an empty region, the conductive material layer being electrically connected to the first conductive region and including a top opening that exposes the empty region; and

forming a conductive cover layer above the contact structure, ~~and covering~~ the cover layer closing the top opening and the empty region, wherein the conductive material layer is formed by steps including:

coating a side surface of the insulating layer, which laterally defines the through opening, with a coating portion of the conductive material layer which laterally defines the empty region; and

forming a horizontal portion of the conductive material layer that extends on top of the insulating layer and beneath the covering layer.

22. (Canceled)

23. (Original) The process of claim 21 wherein the conductive material has a side surface and a bottom surface that faces the first conductive region, and the empty region is surrounded by the conductive material layer.

24. (Canceled)

25. (Original) The process of claim 21 wherein forming the conductive material layer includes depositing a titanium layer on a sidewall of the insulating layer which laterally defines the through opening and depositing a titanium nitride on the titanium layer, the titanium nitride layer laterally defining the empty region.

26. (Original) The process of claim 21 wherein forming the conductive material layer includes depositing a first conductive layer by PVD and depositing a second conductive layer by CVD.

27. (Original) The process of claim 21 wherein the through opening has a width of about 0.18 – 0.35 microns, forming the conductive material layer includes forming a first conductive layer having a thickness between 10 and 100 nm and forming a second conductive layer having a thickness between 50 and 200 nm.

28. (Original) The process of claim 27 wherein the first conductive layer includes titanium and the second conductive layer includes titanium nitride.

29. (Original) The process of claim 21 wherein the integrated device is a ferro-electric memory comprising a transistor and a ferro-electric capacitor; the step of forming a first conductive region comprises forming a first conduction region of the transistor in a substrate of semiconductor material; the step of forming an insulating layer comprises depositing insulating material on top of the substrate, and the step of forming the covering layer includes forming a ferro-electric material region; the process further comprising:

forming a second conductive region between the covering layer and the contact structure, the second conductive region forming a first plate of the ferro-electric capacitor; and

forming a second plate of the ferro-electric capacitor on top of the ferro-electric material region.

30. (New) The process for manufacturing an integrated device according to claim 1, wherein the conductive material layer of the contact structure includes a top portion that extends on top of said insulating layer and the second conductive region extends on top of the top portion of the conductive material layer.

31. (New) The process for manufacturing an integrated device according to claim 30, wherein the second conductive region does not extend into the through opening.

32. (New) The process for manufacturing an integrated device according to claim 11, wherein the conductive material layer includes a top portion that extends on top of said

insulating layer and the second conductive region extends on top of the top portion of the conductive material layer.

33. (New) The process for manufacturing an integrated device according to claim 32, wherein the second conductive region does not extend into the through opening.